Rewrite paragraph [0043] to read as follows:

When (N x D) is larger than the byte capacity of cache memory 100, the outgoing word is mainly stored in main memory 96 and controller 90 uses cache memory 100 to store only as many recently incoming sequence words as it can hold. Thus when controller 90 detects an INPUT_READY signal pulse (step 110) and when (NxD) is larger than the capacity of cache memory 100 (step 112), controller 90 responds to the INPUT_READY pulse by commanding DMA controller 94 to read bytes stored in main memory 96 that are to form the next word of outgoing sequence A. As DMA reads those bytes, controller 90 writes them into appropriate locations of output buffer 102 (step 120). Since not all of the bytes of the outgoing word being assembled in output buffer 102 reside in main memory 96, controller 90 obtains the missing bytes from recently arrived incoming words stored in cache memory 100 and writes them to the appropriate storage locations of output buffer 102 at step 120. After finishing transferring data bytes of the next word of outgoing sequence A from either main memory 96 or cache memory 100 into the output buffer 102, the controller 90 writes the bytes of the incoming sequence word stored in input buffer 92 into the cache memory 100 (step 122). When storing the incoming sequence word, the controller 90 determines whether cache memory 100 has become full (step 124). If so, controller 90 flushes the cache 100 by commanding DMA controller 94 to transfer data bytes stored in cache memory 100 into main memory 96 (step 130) by overwriting bytes that are no longer needed. After flushing cache memory 100, ~~controller 90 c~~ controller 90 stores the remaining bytes of the incoming sequence word into cache memory 100. After storing the incoming sequence word in the cache memory 100, controller 90 pulses the OUTPUT_READY signal (step 132) to signal an external circuit that the next word of output sequence A is available in output buffer 102.